AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions of claims in the application. Claims 3-34, and 36-52 have been amended herein.

1. (Previously presented) A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

a processor interface for interfacing the synchronization apparatus with a host processor;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network; and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor.

2. (Original) The time synchronization apparatus of claim 1, being configurable to operate as one of a synchronization master and a synchronization slave.

3. (Currently amended) The time synchronization apparatus of claim 1, being configured to operate as a synchronization master, ~~wherein~~ the transmitter periodically transmits message frames at a fixed period.

4. (Currently amended) The time synchronization apparatus of claim 3, ~~wherein~~ the fixed period is about 50μs.

5. (Currently amended) The time synchronization apparatus of claim 3, ~~wherein~~ the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval.

6. (Currently amended) The time synchronization apparatus of claim 5, ~~wherein~~ the LCM interval is 600ms.

7. (Currently amended) The time synchronization apparatus of claim 3, being configured as a synchronization master, ~~wherein~~ the transmitter transmits message frames having multiplexed data and direct data.

8. (Currently amended) The time synchronization apparatus of claim 7, ~~wherein~~ the frame comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes.

9. (Currently amended) The time synchronization apparatus of claim 8, ~~wherein~~ the data field comprises 6 32 bit words, and ~~wherein~~ the amount of multiplexed data and the amount of direct data in each message frame is configurable.

10. (Currently amended) The time synchronization apparatus of claim 9, ~~wherein~~ each message frame comprises a direct data portion and a multiplexed data portion, ~~wherein~~ the direct data comprises the direct data portion of a single frame, and ~~wherein~~ the multiplexed data comprises the multiplexed data portions of a plurality of frames.

11. (Currently amended) The time synchronization apparatus of claim 10, ~~wherein~~ the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

12. (Currently amended) The time synchronization apparatus of claim 9, ~~wherein~~ the amount of multiplexed data and the amount of direct data in each message frame is configurable according to information from the host processor.

13. (Currently amended) The time synchronization apparatus of claim 7, ~~wherein~~ the timing system is adjustable according to information received from the host processor.

14. (Currently amended) The time synchronization apparatus of claim 1, being configured as a synchronization slave, ~~wherein~~ the receiver receives message frames at a fixed period, and ~~wherein~~ the timing system is adjusted according to the fixed period.

15. (Currently amended) The time synchronization apparatus of claim 14, ~~wherein~~ the fixed period is about 50μs.

16. (Currently amended) The time synchronization apparatus of claim 14, ~~wherein~~ the receiver receives a message frame having an LCM indicator at a least common multiple (LCM) interval.

17. (Currently amended) The time synchronization apparatus of claim 16, ~~wherein~~ the LCM interval is 600ms.

18. (Currently amended) The time synchronization apparatus of claim 16, ~~wherein~~ the timing system is adjusted according to the LCM indicator.

19. (Currently amended) The time synchronization apparatus of claim 16, ~~wherein~~ the receiver interrupts the host processor according to the LCM indicator.

20. (Currently amended) The time synchronization apparatus of claim 14, ~~wherein~~ the transmitter transmits message frames at the fixed period.

21. (Currently amended) The time synchronization apparatus of claim 20, ~~wherein~~ the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data.

22. (Currently amended) The time synchronization apparatus of claim 21, ~~wherein~~ the message frames comprise a data field with 6 32 bit words, and ~~wherein~~ the amount of multiplexed data and the amount of direct data in each message frame is configurable.

23. (Currently amended) The time synchronization apparatus of claim 22, ~~wherein~~ each message frame comprises a direct data portion and a multiplexed data portion, ~~wherein~~ the direct data comprises the direct data portion of a single frame, and ~~wherein~~ the multiplexed data comprises the multiplexed data portions of a plurality of frames.

24. (Currently amended) The time synchronization apparatus of claim 23, ~~wherein~~ the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

25. (Currently amended) The time synchronization apparatus of claim 24, ~~wherein~~ the receiver presents direct data from received message frames to the host processor at the fixed period.

26. (Currently amended) The time synchronization apparatus of claim 25, ~~wherein~~ the receiver presents multiplexed data from received message frames to the host processor at a multiple of the fixed period.

27. (Currently amended) The time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value from the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, ~~wherein~~ the multiplication result value is the product of the multiplication value and the operand.

28. (Currently amended) The time synchronization apparatus of claim 27, ~~wherein~~ the direct data received in the message frame comprises the operand.

29. (Currently amended) The time synchronization apparatus of claim 14, ~~wherein~~ the message frame comprises a status component indicative of the status of an upstream device, ~~wherein~~ the receiver provides the status component to the host processor.

30. (Currently amended) The time synchronization apparatus of claim 14, ~~wherein~~ the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

31. (Currently amended) The time synchronization apparatus of claim 30, ~~wherein~~ at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, ~~wherein~~ the direct data from a received message frame is passed through to the transmitter.

32. (Currently amended) The time synchronization apparatus of claim 30, comprising a multiplier, ~~wherein~~ at least a portion of the direct data in the message frames transmitted by the transmitter comprises a multiplication result value provided to the transmitter by the multiplier.

33. (Currently amended) The time synchronization apparatus of claim 30, ~~wherein~~ at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

34. (Currently amended) The time synchronization apparatus of claim 33, ~~wherein~~ the multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

35. (Original) The time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain.

36. (Currently amended) The time synchronization apparatus of claim 35, ~~wherein~~ the receiver receives message frames at a fixed period, and ~~wherein~~ the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

37 (Currently amended) The time synchronization apparatus of claim 36, ~~wherein~~ at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, ~~wherein~~ the direct data from a received message frame is passed through to the transmitter.

38. (Currently amended) A synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

a host processor in communication with the first controller via a backplane bus in the control chassis;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network;

a timing system ~~with~~ including a clock ~~and maintaining~~ that maintains an indication of time according to information received from one of the network and the host processor; and

a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave.

39. (Currently amended) A synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

a processor interface for interfacing the synchronization circuit with a host processor;

a transmitter component adapted to transmit synchronization information and data to a network in the control system;

a receiver component adapted to receive synchronization information and data from the network; and

a timing system ~~with~~ including a clock ~~and maintaining~~ that maintains an indication of time according to information received from one of the network and the host processor,

~~wherein~~ the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.

40. (Currently amended) The system of claim 39, ~~wherein~~ the transmitter component periodically transmits message frames comprising direct data, and ~~wherein~~ the direct data is obtained from at least one of the receiver component and the host processor.

41. (Currently amended) The system of claim 39, further comprising a multiplier, ~~wherein~~ the transmitter component periodically transmits message frames comprising direct data, and ~~wherein~~ the direct data is obtained from at least one of the receiver, the host processor, and the multiplier.

42. (Currently amended) The system of claim 39, ~~wherein~~ the transmitter component periodically transmits message frames comprising multiplexed data, and ~~wherein~~ the multiplexed data is obtained from the host processor.

43. (Currently amended) The system of claim 39, ~~wherein~~ the transmitter component periodically transmits message frames comprising direct data and multiplexed data, and ~~wherein~~ the amount of the multiplexed data in the message frames and the amount of direct data in the message frames is configurable.

44. (Currently amended) The system of claim 39, ~~wherein~~ the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and ~~wherein~~ the synchronization circuit provides at least one of received direct data, received multiplexed data, and received status information from the receiver component to the host processor.

45. (Currently amended) The system of claim 44, further comprising a multiplier operating on the received direct data, and ~~wherein~~ the synchronization circuit provides a multiplier result value from the multiplier to the host processor.

46. (Currently amended) The system of claim 45, ~~wherein~~ the synchronization circuit provides a multiplication value to the multiplier from the host processor.

47. (Currently amended) The system of claim 44, ~~wherein~~ the status information comprises at least one of status of an upstream device, and an error counter.

48. (Currently amended) The system of claim 39, ~~wherein~~ the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and ~~wherein~~ the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor.

49. (Currently amended) The system of claim 39, ~~wherein~~ the transmitter component periodically transmits message frames having synchronization information, ~~wherein~~ the synchronization information is obtained from the timing system, and ~~wherein~~ the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor.

50. (Currently amended) The system of claim 39, ~~wherein~~ the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver.

51. (Currently amended) The system of claim 39, ~~wherein~~ the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor.

52. (Currently amended) A synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

means for interfacing the synchronization circuit with a host processor;

means for transmitting synchronization information and data to a network in the control system;

means for receiving synchronization information and data from the network; and

means for maintaining an indication of time according to information received from one of the network and the host processor, ~~wherein~~ the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.